

A Tailed Tent Map Chaotic Circuit Exploiting S²I Memory Elements

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Abstract

In the implementation of discrete time chaotic systems, designers have mostly focused on the choice and synthesis of suitable nonlinear blocks, while correct and fast operation cannot neglect analog memory elements. Herein, a realization exploiting the Tailed Tent Map coupled with S²I sample and hold stages is proposed. Interfacing problems between the memory and the processing sub-circuits are tackled and the possibility to obtain a fivefold speed improvement with respect to previously reported results is demonstrated by means of SPICE and other computer aided simulations.

1 Introduction

Several applications of chaotic hardware (like in secure communication schemes [1], noise generation, stochastic neural models [2], EMI reduction, etc.) can exploit even the simplest kind of chaotic systems, namely a one-dimensional map (Figure 1). Although for obtaining chaotic behavior

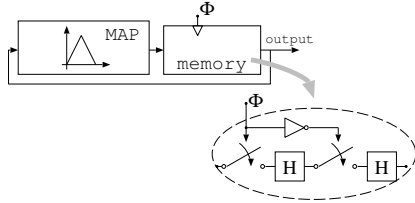


Figure 1: Basic scheme for a one-dimensional chaotic system. A memory element (cascade of two sample-and-hold stages) maintains the input of the map circuit stable during signal processing.

this arrangement requires a fully *analog* signal path, this does not prevent practical and compact CMOS realizations [3–5]. Indeed, interest in these systems has recently grown, mainly focusing on how to obtain useful statistical properties, on the design strategies, and on robustness issues [5].

*This is a pre-print version of a paper presented at the 1999 European Conference on Circuit Theory and Design (ECCTD '99). Published paper available in "ECCTD '99: Proceedings of the 1999 European Conference on Circuit Theory and Design", European Circuit Society (ECS) 1999. Cite as:

S. Callegari, R. Rovatti, G. Setti, "A tailed tent map chaotic circuit exploiting S²I memory elements", in Proc. of ECCTD'99, vol. 1, Stresa, IT, Sep. 1999, pp. 193–196.

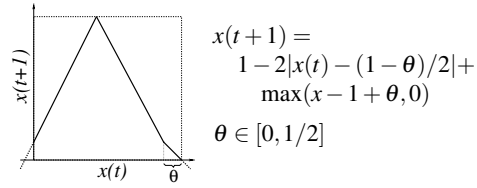


Figure 2: The Tailed Tent Map.

In other words, the attention has been mainly devoted to the choice of suitable nonlinear maps and on their synthesis.

However, for truly effective operation, *all* the elements in the signal path (thus including the analog memory in the feedback loop) must be optimized having the requirements of a chaotic system in mind.

Recently, investigation in this direction has been proposed for a representative set of systems defined by piecewise-affine (PWA) maps and characterized by a uniform invariant probability density function (PDF) of the generated samples [6]. Two results of such investigation are that even maps which are traditionally considered robust with respect to implementation inaccuracies suffer from S/H errors and that, among all these errors, signal dependent ones seem to be the most critical.

Herein, we propose a system based on the most robust map among those considered in [6] — the Tailed Tent Map (TTM) (Figure 2) [5] — coupled with one of the analog memory schemes which best address the signal dependent error issue, i.e. the S²I technology [7]. Not surprisingly, this allows to significantly relax the cycle time limitations and to improve the performance achievable with respect to previously presented results.

The system is designed with a standard 0.8μm *n-well* CMOS technology and allows an operating frequencies of at least 5MHz — which stands out with regard to around 750kHz in [5]. This is obtained at a very good level of esteemed accuracy and with internal currents as low as ±25μA, for low-power operation.

2 Building blocks and interfacing

The abstract elements illustrated in Figure 1 are herein better investigated to illustrate the adoption of S²I and how consequent interfacing issues are tackled.

2.1 The Nonlinear map

The most common choice for designing PWA maps is the current mode approach. Figure 3 shows a framework in which *current splitters* are used to introduce breakpoints by operating as unidirectional devices. Splitters are arranged to operate in parallel to reduce propagation times.

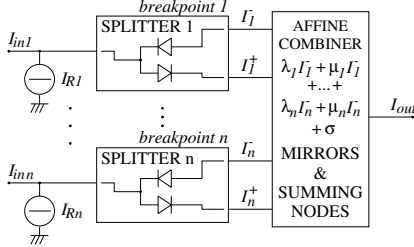


Figure 3: General PWA current-mode architecture.

The affine-combiner is implemented by means of mirrors and summing nodes. A splitter is required for every breakpoint, so that the TTM requires two of them (and two input currents).

The splitters/combiner pair is a potential bottleneck for high frequency operation since mirror transistors cannot be taken minimal size, as this would deteriorate their matching properties and the mirrors accuracy [8]. As a consequence, the extra-capacitance that has to be driven dictates very careful design. The proposed TTM circuit (Figure 4) follows

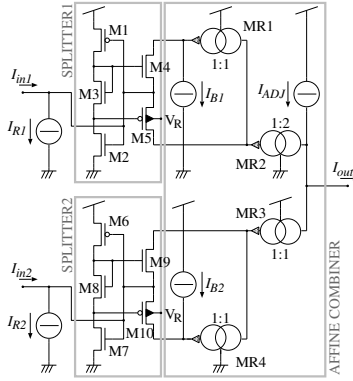


Figure 4: The Tailed Tent Map circuit.

the current trend of adopting active splitters [3]. Exploiting an amplifier (M1-M2-M3 or M6-M7-M8), rather than simply adopting diodes or current mirrors [4] reduces the splitter input impedance, speeding up the system response which is commonly dominated by the product between input impedance and input capacitance. With regard to established designs (see e.g. [3]), three modifications are proposed:

i. **the adoption of transistors M3 and M8**, bringing the input impedance further down by assuring that the voltage swing at the input capacitance is never larger than

$$\frac{V_{T_n} + V_{\text{eff}_N} + |V_{T_p}| + |V_{\text{eff}_P}| - V_{T_D} - V_{\text{eff}_D}}{k} \quad (1)$$

where V_{T_n} is the threshold voltage of M4 (or M9), V_{eff_N} is its driving voltage, V_{T_p} is the threshold voltage of M5 (or M10), V_{eff_P} is its driving voltage, V_{T_D} is the threshold voltage of transistor M3 (or M8), V_{eff_D} is the diode driving voltage and k is the gain of the inverting amplifier M1-M2-M3 (or M6-M7-M8);

ii. **the adoption of a dummy splitter** driven by no current (Figure 5) in order to generate a reference voltage V_R

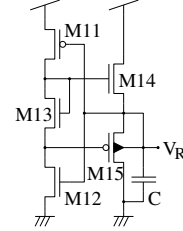


Figure 5: The dummy splitter used to generate V_R .

to be applied to the well of the PMOS transistors M5 and M10. This avoids body effect, reduces V_{T_p} in (1), and loads no extra capacitance on the input node as a well-source connection would do. If a twin well technology is available, it is convenient to tie also the bulks of M4 and M9 to V_R ;

iii. **the adoption of bias currents**, I_{B1} and I_{B2} , pumped into mirrors MR1 and MR4 to make sure that in no condition there are mirrors copying a null current. In fact, the step response time of a current mirror is mostly dependent on the step final current and grows very rapidly as this approaches zero.

As it will be seen in §2.3, the search for low input impedance is not just a matter of speed, but also of interfacing to S^2I stages, so that the extra hardware required for the dummy splitter is effectively justified. Note also that the mirrors require cascode structures in order to minimize inaccuracies due to channel length modulation and finite output impedance. High-swing cascodes are suggested, as they have a limited hardware cost and they allow the stacking of the splitters and the mirrors at a power supply of 5 V. For suitable matching, gate areas of mirroring transistors must be no less than $50\mu\text{m}^2$ to $60\mu\text{m}^2$ [8]. Finally, consider that reference currents I_{R1} and I_{R2} and the offset cancelling current I_{ADJ} can be selected among a range of values, with the result of changing the map invariant set. This degree of freedom will also be exploited in §2.3.

2.2 The S^2I analog memory element

The memory element required for map iteration must transfer instantaneously the value at its input to the output when triggered by a clocking event, and at no time instant is allowed to become transparent. To achieve this, it is realized in a master-slave fashion cascading two sample-and-hold (S/H) circuits driven by opposite clock phases (balloon in Figure 1).

In its simplest realization, an S^2I S/H (or dynamic current mirror) [7] is represented in Figure 6. Its working principle is based on a *two step sampling* of the input current. First

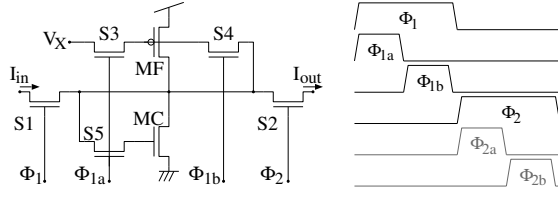


Figure 6: Basic S²I circuit and timings. Grayed out clock phases Φ_{2a} and Φ_{2b} would be used by an identical cascaded unit.

of all, MC samples the input current plus a certain reference current I_X generated by MF, whose gate is connected to a reference voltage V_X (phase Φ_{1a}). After this first *coarse* sampling, the current on MC is $I_{in} + I_X + \epsilon_C$ where ϵ_C is an error mainly due to clock feed-through on switch S5. In the second step, MF samples the difference between the input current and the current stored on MC, i.e. $I_X + \epsilon_C$ (phase Φ_{1b}). Phase Φ_2 is the *hold* phase. Also at the end of the *fine* sampling Φ_{1b} an error is committed, so that the final current stored on MF is $I_X + \epsilon_C - \epsilon_F$. Hence, the output current of the S²I S/H is $I_{in} + \epsilon_F$.

With this, even though an S²I S/H stage is not immune from sampling errors, the error ϵ_F is introduced while sampling a current always very close to I_X so to be an (almost) signal independent error.

Moreover, a whole memory element is made of two S/H stages. In the case of S²I stages, two identical units can be directly cascaded, thanks to the presence of the reference current I_X which makes an S²I S/H capable of dealing with both positive and negative input currents. This arrangement has the property of cancelling signal independent errors [9], so that the operation of a S²I 2 stage memory element is (theoretically) error free.

Note that, for cascading, the down-hill unit requires clocking signals complementary to those used in the up-hill one: in Figure 6, signals Φ_2 , Φ_{2a} and Φ_{2b} are meant to drive the second S/H. Clock phases are rigorously non-overlapping.

2.3 Interfacing

This section deals with the problem of interfacing a TTM circuit (§2.1) to an S²I memory element.

First of all, electrical interfacing will be considered. S²I circuits do not pose particular requirements to units driving them, but *do* pose constraints on the circuits being driven by them, since they are fundamentally designed to be cascaded to other S²I units. This is evident if one looks at the absence of cascode stages replacing over MC and MF, which may therefore be affected by channel length modulation. Errors are prevented by the fact that when an S²I unit is cascaded to another identical one, the fine sampling phase of the second unit guarantees the voltage at the drains of MC and MF to be approximately V_X , i.e. the same voltage as at the end of the first unit sampling.

To prevent channel modulation error when driving a non-S²I stage without having to provide cascode structures for

MC and MF, we need to adjust the input voltage of the circuit being driven by the down-hill S²I stage to be *constantly* as similar as possible to the V_X used as a reference in the S²I circuits. To do so, a very low input impedance is needed.

Connecting to conventional mirrors is thus generally not feasible due to their non-negligible input impedance. What we propose is instead to connect the S²I memory element directly to the TTM circuit. In fact, this block has been designed for an extremely low input impedance (§2.1) and for an input voltage almost fixed at V_R . The dummy splitter already introduced in §2.1 is here of great help as it can be exploited to generate $V_X \equiv V_R$.

The second point is functional interfacing. The TTM circuit requires two input currents. Furthermore, an additional current is necessary to read the output of the overall chaotic system. To cope with this, we propose to build current mirrors *inside* the S²I memory element. The final, complete circuit is shown in Figure 7. Such a circuit can be connected

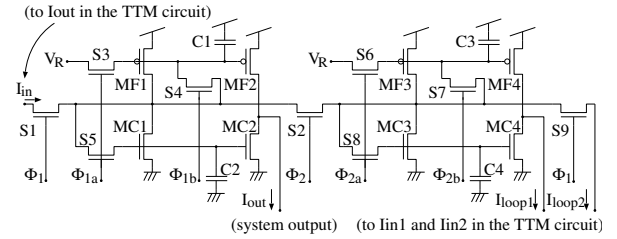


Figure 7: A S²I memory element that can be directly interfaced with the TTM circuit shown in Figure 4.

to the TTM circuit exploiting input I_{in} and outputs I_{loop1} and I_{loop2} . I_{out} is for reading the overall chaotic system output: it offers a time shifted (half clock cycle), complemented version of the system state variable. In the whole circuit this is the only signal subject to a non-compensated sampling error (which happens to be a constant offset not particularly troublesome for most applications). Note that mirroring inside the S²I subsystem introduces matching errors (which would anyway be introduced elsewhere in the signal path). To keep them low, all the MCx and the MFx transistors must be sized to have an area greater than $50\mu\text{m}^2$ to $60\mu\text{m}^2$. The consequence is a noticeable sampling error due to charge feed-through on the drain-to-gate capacitances of MCx and the MFx. Nonetheless proper device dimensioning can keep such error tolerable as confirmed by the the results in §3.

As a further consideration, note that sampling error may also be reduced by exploiting the ability of S²I S/H to cope with either positive or negative inputs and adopting a signal range centered on zero. In fact, this allows to use the smallest possible reference currents, to which errors are tied.

To do so, the values of I_{R1} , I_{R2} and I_{ADJ} can be chosen so that the system invariant set is centered around zero. The circuit has been simulated with $I_{R1} = -1.25\mu\text{A}$, $I_{R2} = 22.5\mu\text{A}$, $I_{B1} = I_{B2} = 2.5\mu\text{A}$ and $I_{ADJ} = 32.5\mu\text{A}$, so that the “state variable” currents are in the $\pm 25\mu\text{A}$ range.

Finally, we shall briefly consider timings. Being the S²I dynamic mirror a sample-and-hold rather than a track-and-hold unit, it cannot deliver output while sampling. Hence,

only half of clock cycle is left to the map circuit to elaborate its output (see Figure 8). While this poses constraints on the response time of the map circuit, it might (at least theoretically) allow interleaving of two analog memory elements on the same TTM circuit.

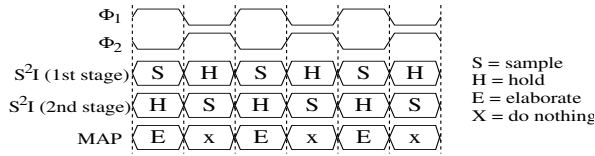


Figure 8: Basic timings of the overall TTM+S²I system.

3 System simulation and conclusions

System simulations were run using SPECTRE, referring to charge-conservative BSIM3 device models. Figure 9 shows

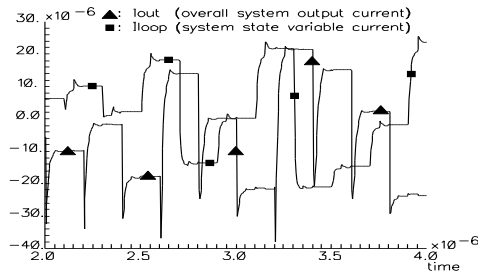


Figure 9: A chaotic sequence as obtained by the overall system. Both the output current and the “state variable” current are shown.

a collection of output samples as produced by the overall system. The operating frequency of 5MHz is limited by the worst-case step response time of the TTM circuit (about 90ns — Figure 10) which corresponds to a step in the input current taking a splitter right over or below threshold.

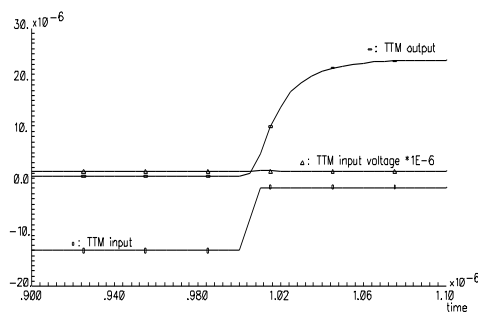


Figure 10: Worst case switching of the TTM circuit. Traces show the input current, the output current and the voltage at one of the TTM inputs, confirming the low input impedance of the circuit.

To obtain a reliable estimation of the asymptotic statistical distribution of the system states in a reasonable amount

of time, we have simulated the behavior of an open-loop system based on the TTM circuit together with the S²I subsystem, driven by a stepping signal spanning the whole range of operation of the TTM circuit (.TRAN analysis). Successively, the collected information has been used to build and interpolating behavioural model in C code. Finally, this efficient model has been iterated to produce the large number of samples required for PDF estimation. The result is reported in Figure 11 to show a good agreement with the theoretical expectations.

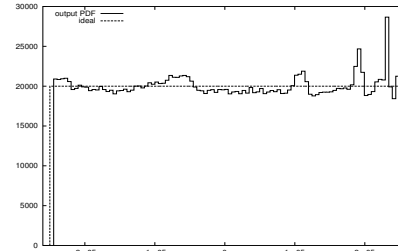


Figure 11: PDF of the system simulated using C code and an approximation of the open-loop behavior. Offsets are due to the fact that the output is subject to signal independent errors.

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